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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH  
121 S. 8TH STREET  
SUITE 1600  
MINNEAPOLIS, MN 55402

EXAMINER

KROFCHECK, MICHAEL C

|          |              |
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2186

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/767,555

Applicant(s)

CHOI ET AL.

Examiner

Michael Krofcheck

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-34 and 36-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-34 and 36-38 is/are rejected.
- 7) ☒ Claim(s) 2, 6, 10, 14, 16, 19, 23, 25, 27, 30 and 33 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 January 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>3/24/2006</u> .   | 6) <input type="checkbox"/> Other: _____                                    |

### **DETAILED ACTION**

1. This office action is in response to application 10/767,555 filed on 1/29/2004.
2. Claims 1-34, 36-37 have been submitted for examination.
3. Claims 1-34, 36-37 have been examined.

### ***Drawings***

4. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

5. Claims 2, 6, 10, 14, 16, 19, 23, 27, 30, 33 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The parent claims of the claims objected to claim a memory device. The dependent

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claims cited above state, "wherein the memory device comprises a device selected from the group consisting of...a volatile memory device, a non-volatile memory device..." A memory device must be either volatile or non-volatile. As such, since the claim states the group contains all memory devices, it does not further limit its parent claim.

6. Claim 25 objected to because of the following informalities:

a. There should be a space between the number 24 and the word, 'wherein'.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 13, 20, 26, 34, 38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claims 13, 20, 26 recite the limitation "the first and second edges of the clock signal" in each claim. There is insufficient antecedent basis for this limitation in the claim. There is no prior mention of a second edge. Does the applicant mean the first edge of the first/second cycle? Should these claims be similar to claim 9 which is related to the first/second clock cycle?

10. Claims 34 and 38 recites the limitation "the timing signal" in four locations in each claim. There is insufficient antecedent basis for this limitation in the claim. Does the applicant mean, the clock cycle?

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11. Additionally, claims 34 and 38 are indefinite and confusing because the statement of, "wherein the command and address signals [during the clock cycle of the clock signal] are selected from the group consisting of initiating the command and address signals..." This statement leads the reader to believe that the group is going to be a group of different command and address signals. However, in actuality the "group" is just a number of different ways that the address and command signals are initiated with respect to a clock signal. Instead of saying that they are "selected from the group", the applicant needs to somehow say that they are *initiated* in one or more of the multiple ways listed.

***Claim Rejections - 35 USC § 102***

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1-4, 8-10, 15-38, rejected under 35 U.S.C. 102(b) as being anticipated by DeMone et al., US patent 6266750.

14. With respect to claim 1, DeMone teaches of a method of operating a memory device, comprising: receiving a first subset of a set of command and address signals substantially simultaneous with receiving a first edge of a clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5);

receiving a second subset of the set of command and address signals substantially simultaneous with receiving a second edge of the clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5); and

performing a memory command in response to the set of command and address signals (fig. 5a, column 5, lines 10-32).

15. With respect to claim 8, Demone teaches of a method of operating a memory device, comprising: receiving a first subset of a set of command and address signals substantially simultaneous with receiving a first edge of a first cycle of a clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; packets A0-A1);

receiving a second subset of a set of command and address signals substantially simultaneous with receiving a first edge of a second cycle of a clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; packets A2-A3); and

performing a memory command in response to the set of command and address signals (fig. 5a, column 5, lines 10-32).

16. With respect to claim 15, Demone teaches of a memory device comprising: multiple command and address pins to receive a first subset of a set of command and address signals substantially simultaneous with receiving a first edge of a clock signal, wherein the multiple command and address pins to further receive a second subset of the set of command and address signals substantially simultaneous with receiving a second edge of a clock signal (fig. 1, 3a-b; column 3, lines 20-30; column 3, lines 44-51; column 3, line 61-column 4, line 5; as the SLDRAM is an IC (integrated circuit), there must be I/O pins connecting to the command link to enable the signals to be received

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from the command module as described. As there are 10 command/address lines, there must be 10 pins), and

wherein the memory device operates to perform a memory command in response to the set of received command and address signals (fig. 5a, column 5, lines 10-32).

17. With respect to claim 18, Demone teaches of a memory device comprising: multiple command and address pins to receive a first subset of a set of command and address signals substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein the multiple command and address pins to further receive a second subset of the set of command and address signals substantially simultaneous with receiving a first edge of a second cycle of the clock signal (fig. 1, 3a-b; column 3, lines 20-30; column 3, lines 44-51; column 3, line 61-column 4, line 5; as the SLDRAM is an IC (integrated circuit), there must be I/O pins connecting to the command link to enable the signals to be received from the command module as described with respect to claim 8. As there are 10 command/address lines, there must be 10 pins), and

wherein the memory device to perform a memory command in response to the set of received command and address signals (fig. 5a, column 5, lines 10-32).

18. With respect to claim 21, Demone teaches of a memory circuit comprising: one or more integrated circuit memory devices operable for communicating with an external controller (fig. 1; column 3, lines 20-30; where the SLDRAMs are individual ICs (integrated circuits) connected to a command module),

wherein each of the integrated circuit memory devices operates to receive a first subset of a set of command and address signals substantially simultaneous with receiving a first edge of a clock signal, wherein each of the integrated memory circuit devices operates to receive a second subset of the set of command and address signals substantially simultaneous with receiving a second edge of a clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5), and

wherein each integrated circuit memory device operates to perform a memory command in response to the set of received associated command and address signals (fig. 5a, column 5, lines 10-32).

19. With respect to claim 24, Demone teaches of a memory circuit comprising: one or more integrated circuit memory devices operable for sending and receiving signals (fig. 1; column 3, lines 20-30; where the SLDRAMs are individual ICs (integrated circuits)),

wherein each of the integrated circuit memory devices operates to receive a first subset of a set of command and address signals substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein each of the integrated memory circuit devices operates to further receive a second subset of the set of command and address signals substantially simultaneous with receiving a first edge of a second cycle of the clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; where the first subset comprises packets A0-A1 and the second subset comprises packets A2-A3), and

wherein each integrated circuit memory device operates to perform a memory command in response to the set of received associated command and address signals received (fig. 5a, column 5, lines 10-32).

20. With respect to claim 28, Demone teaches of a system comprising: one or more integrated circuit memory devices, wherein each of the one or more integrated circuit memory devices includes multiple data, command, and address pins (fig. 1; column 3, lines 20-30; column 4, lines 28-35; where the SLD RAMs are individual ICs (integrated circuits). As the ICs must be able to connect to the command link and data links, they each must have pins that provide electrical connectivity from the desired location, through the ICs' housing to the circuitry. Since there are 10 individual command/address lines (10 bits) there must be 10 pins); and

a bus, wherein the one or more integrated circuit memory devices are coupled via the bus to a controller through the multiple data, command, and address pins (fig. 1, 2a; column 3, lines 20-35, column 4, lines 28-35; where the data links connect the memory devices to the command module. They must be connected through the pins in the IC),

wherein the controller operates to send command and address signals during a clock cycle of a clock signal such that the number of command and address signals sent from the controller to the integrated circuit memory device is higher than a given number of command and address pins in each integrated circuit memory device (fig. 3a-b; column 3, lines 20-30, lines 44-51; column 3, line 61-column 4, line 5; column 4, lines 28-35; there are 4 consecutive 10-bit packets that are received and then combined into

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a 40-bit packet; The signals of 4 packets cannot be transmitted at the same time as there are only 10 bits worth of lines and pins).

21. With respect to claim 32, Demone teaches of a semiconductor circuit comprising: one or more integrated circuit memory devices, wherein each integrated circuit memory device comprises multiple command and address pins, wherein the command and address pins of each integrated circuit memory device are coupled to receive command and address signals (fig. 1; column 3, lines 20-30; column 4, lines 28-35; where the SLDRAMs are individual ICs (integrated circuits). As the ICs must be able to connect to the command link and data links, they each must have pins that provide electrical connectivity from the desired location, through the ICs' housing to the circuitry. Since there are 10 individual command/address lines (10 bits) there must be 10 pins),

wherein the memory devices operates to receive command and address signals during a clock cycle of a clock signal such that the number of command and address signals sent to each integrated circuit memory device is higher than the multiple command and address pins available in each integrated circuit memory device (fig. 3a-b; column 3, lines 20-30, lines 44-51; column 3, line 61-column 4, line 5; column 4, lines 28-35; there are 4 consecutive 10-bit packets that are received and then combined into a 40-bit packet; The signals of 4 packets cannot be transmitted at the same time as there are only 10 bits worth of lines and pins).

22. With respect to claim 36, Demone teaches of a memory circuit comprising: one or more integrated circuit memory devices, wherein each integrated circuit memory device comprises a predetermined number of command and address pins (fig. 1;

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column 3, lines 20-30; column 4, lines 28-35; where the SLD RAMs are individual ICs (integrated circuits). As the ICs must be able to connect to the command link and data links, they each must have pins that provide electrical connectivity from the desired location, through the ICs' housing to the circuitry. Since there are 10 individual command/address lines (10 bits) there must be 10 pins. Since the number of pins is decided before fabrication of the IC, the quantity of 10 corresponding to each command/address line must have been predetermined),

wherein each integrated circuit memory device is coupled to send and receive signals on the predetermined number of command and address pins, wherein the one or more memory devices operates to receive a number of command and address signals during more than one edge of a clock signal such that the number of command and address signals for each integrated circuit memory device are substantially higher than the predetermined number of command and address pins in each integrated circuit memory device (fig. 3a-b; column 3, lines 20-30, lines 44-51; column 3, line 61-column 4, line 5; column 4, lines 28-35; there are 4 consecutive 10-bit packets that are received and then combined into a 40-bit packet; The signals of 4 packets cannot be transmitted at the same time as there are only 10 bits worth of lines and pins).

23. With respect to claims 2, 10, 16, 19, 23, 27, 30, 33, Demone teaches of wherein the memory device comprises a device selected from the group consisting of a DRAM device, a flash memory device, a volatile memory device, a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device (fig. 1-2;

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column 3, lines 20-42; the memory device is a SLD RAM which is a type of DRAM which is classified as volatile memory).

24. With respect to claim 3, Demone teaches of sending the first subset of the set of command and address signals substantially simultaneous with sending the first edge of the clock signal by an external controller; and sending the second subset of the set of command and address signals substantially simultaneous with sending the second edge of the clock signal by the external controller (fig. 1, 2a, 3b; column 3, lines 22-30; column 3, line 61-column 4, line 5; where the command module sends the command/address signals and the clock signal).

25. With respect to claims 4 and 29, Demone teaches of in sending, the external controller is a device selected from the group consisting of a DRAM controller, a central processing unit (CPU), a graphics processing unit (GPU), and a processor (fig. 1; column 3, lines 22-30; as the command module, implemented by a memory controller, controls a type of DRAM, it must be a DRAM controller).

26. With respect to claims 9, and 25, Demone teaches of wherein, in receiving the second subset of command and address signals, the second cycle is substantially subsequent to the first cycle (fig. 3b; column 3, line 61-column 4, line 5).

27. With respect to claims 17, and 22, Demone teaches of wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic

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level "zero", respectively (fig. 3b; column 3, lines 44-51; column 3, line 61-column 4, line 5).

28. With respect to claims 20, and 26, Demone teaches of wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively (fig. 3b; column 3, lines 44-51; column 3, line 61-column 4, line 5).

29. With respect to claim 31, Demone teaches of wherein the controller is operable for sending the command and address signals during the clock cycle of the clock signal comprises sending the command and address signals upon both rising and falling edges of the clock cycle when transferring data to and from each integrated circuit memory device (fig. 3b; column 3, lines 44-51; column 3, line 61-column 4, line 5).

30. With respect to claims 34 and 38, Demone teaches of wherein the command and address signals during the clock cycle of the clock signal is selected from the group consisting of initiating the command and address signals upon both the rising and falling edges of the clock cycle of the clock signal, initiating the command and address signals upon a rising edge of the clock cycle and further initiating address signals on a falling edge of the timing cycle, initiating the command and address signals upon two consecutive rising edges of the timing signal, and initiating the command and address signals on a rising edge of the timing cycle and further initiating the address signals on a

subsequent rising edge of the timing cycle (fig. 3b; column 3, lines 44-51; column 3, line 61-column 4, line 5).

31. With respect to claim 37, Demone teaches of wherein the integrated circuit memory device is a DRAM device (fig. 1; column 3, lines 20-30; where the IC is a SLDRAM a type of DRAM).

32. Claims 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Merritt, US patent 6192002.

33. With respect to claim 8, Merritt teaches of a method of operating a memory device, comprising: receiving a first subset of a set of command and address signals substantially simultaneous with receiving a first edge of a first cycle of a clock signal (fig. 3; column 5, lines 12-17);

receiving a second subset of the set of command and address signals substantially simultaneous with receiving a first edge of a second cycle of the clock signal (fig. 3; column 5, lines 12-17); and

performing a memory command in response to the set of command and address signals (fig. 3; column 5, lines 44-53).

34. With respect to claim 9 Merritt teaches of wherein, in receiving the second subset of command and address signals, the second cycle is substantially subsequent to the first cycle (fig. 3; column 5, lines 12-17).

35. With respect to claim 10, Merritt teaches of wherein the memory device comprising a device selected from the group consisting of a DRAM device, a flash memory device, a volatile memory device, a non-volatile memory device, a static

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random access memory (SRAM) device, and a static memory device (fig. 1-2; column 3, lines 5-7; where the memory device is a SDRAM, a type of DRAM, which is classified as volatile memory).

36. Claims 11-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohshima et al, US patent application publication 2001/0006483.

37. With respect to claim 11, Ohshima teaches of a method of operating a memory device, comprising: receiving a set of command signals and a first subset of a set of address signals substantially simultaneous with receiving a first edge of a first cycle of a clock signal (fig. 17, paragraph 0084; RDA (read command) and UA (upper address) are received on the first cycle);

receiving a second subset of the set of address signals substantially simultaneous with receiving a first edge of a second clock cycle of the clock signal (fig. 17, paragraph 0084; LA (lower address) is received on the second cycle); and

performing a memory command in response to the set of command and address signals (fig. 16-17, paragraph 0085; where the readout operation enhances the access time tRAC, reading out the data packets (Q0, Q1) quicker).

38. With respect to claim 12, Ohshima teaches of wherein, in receiving the second subset of the set of address signals, the second cycle is substantially subsequent to the first cycle (fig. 17, paragraph 0084).

39. With respect to claim 13, Ohshima teaches of wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level

"one" and a transition from the logic level "one" to the logic level "zero", respectively (fig. 17, paragraph 0084).

40. With respect to claim 14, Ohshima teaches of wherein the memory device comprising a device selected from the group consisting of a DRAM device, a flash memory device, a volatile memory device, a non-volatile memory device, a static random access operating memory (SRAM) device, and a static memory device (paragraph 0058; where the memory is a FCRAM (fast cycle RAM) a volatile memory device).

### ***Claim Rejections - 35 USC § 103***

41. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

42. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

43. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

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the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

44. Claims 18-20 are 24-27 rejected under 35 U.S.C. 103(a) as being unpatentable over Merritt and Ryan, US patent 6172893.

45. With respect to claim 18, Merritt teaches of receiving a first subset of a set of command and address signals substantially simultaneous with receiving a first edge of a first cycle of a clock signal (fig. 3; column 5, lines 12-17),

further receiving a second subset of the set of command and address signals substantially simultaneous with receiving a first edge of a second cycle of the clock signal (fig. 3; column 5, lines 12-17), and

wherein the memory device to perform a memory command in response to the set of received command and address signals (fig. 3; column 5, lines 44-53).

Ryan teaches of multiple command and address pins to receive multiple command and address packets (figs. 1a-2; column 2, lines 26-30).

Merritt and Ryan are analogous arts as they are both in the same field of endeavor, Memory accessing. It would have been obvious to one of ordinary skill in the art having the teachings of Merritt and Ryan at the time of the invention to include the command and address pins of Ryan in the memory of Merritt to receive the command

and address signals. Their motivation would have been to allow for the memory device to be easily mounted into a printed circuit board.

46. With respect to claim 24, Merritt teaches of a memory circuit comprising: one or more memory devices operable for sending and receiving signals, wherein each of the memory devices operates to receive a first subset of a set of command and address signals substantially simultaneous with receiving a first edge of a first cycle of a clock signal (fig. 3; column 5, lines 12-17),

wherein each of the memory devices operates to further receive a second subset of the set of command and address signals substantially simultaneous with receiving a first edge of a second cycle of the clock signal (fig. 3; column 5, lines 12-17), and

wherein each memory device operates to perform a memory command in response to the set of received associated command and address signals received (fig. 3; column 5, lines 44-53).

Ryan teaches of memory devices being generally fabricated as an integrated circuit (column 8, lines 43-46).

Merritt and Ryan are analogous arts as they are both in the same field of endeavor, Memory accessing. It would have been obvious to one of ordinary skill in the art having the teachings of Merritt and Ryan at the time of the invention to implement the memory of Merritt as an integrated circuit as taught in Ryan as it is commonly done in the art, Ryan column 8, lines 43-53.

47. With respect to claims 19, and 27, Merritt teaches of the limitations cited with respect to claim 10 above.

48. With respect to claims 20, and 26, Merritt teaches of wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively (shown in fig. 3).

49. With respect to claim 25, Merritt teaches of the limitations cited with respect to claim 9 above.

50. Claims 5-7 rejected under 35 U.S.C. 103(a) as being unpatentable over Ohshima and Pawlowski, US patent 5973989.

51. With respect to claim 5, Ohshima teaches of a method of operating a memory device, comprising: receiving a set of command signals and a first subset of a set of address signals substantially simultaneous with receiving a first edge of a clock signal (fig. 17, paragraph 0084; RDA (read command) and UA (upper address) are received on the first edge);

receiving a second subset of the set of address signals substantially simultaneous with receiving a second clock signal (fig. 17, paragraph 0084; LA (lower address) is received on the second cycle); and

performing a memory command in response to the set of command and address signals (fig. 16-17, paragraph 0085; where the readout operation enhances the access time t<sub>RAC</sub>, reading out the data packets (Q0, Q1) quicker).

Pawloski teaches of sending control signals for accessing a memory at the rising and falling edge of the clock signal (abstract).

Ohshima and Pawlowski are analogous arts as they are both in the same field of endeavor, memory accessing. It would have been obvious to one of ordinary skill in the art having the teachings of Ohshima and Pawlowski at the time of the invention to transmit the signals on the rising and falling edges of the clock cycle in Ohshima as taught in Pawlowski. Their motivation would have been to transmit data at a high frequency to the memory (Pawlowski, column 2, lines 25-30).

52. With respect to claim 6, Ohshima teaches of the limitations cited above with respect to claim 14.

53. With respect to claim 7, Ohshima teaches of limitations cited above with respect to claim 13.

### ***Conclusion***

54. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

55. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

56. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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57. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Michael C. Krofcheck



MATTHEW KIM  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100